

## **REMARKS**

Claims 1-45 are pending in the present application. claims 7-13, 15-17, 19, 22-29 and 31-40 have been withdrawn. Claim 14 has been rejected under § 102(e) as being anticipated by Nalbantis (US 2004/0148553). Claims 1, 14, 18, 30, and 45 have been rejected under § 103 as being unpatentable by Blake et al. (US 6,847,904) (Blake). Claims 2, 41 and 42 have been rejected under § 103 as being unpatentable by Blake in view of Nalbantis. Claims 3-4, 20 and 43-44 have been rejected under § 103 as being unpatentable by Blake in view of Nalbantis and further in view of Tomasz (US 6,400,416). Claims 5-6 have been rejected under § 103 as being unpatentable by Blake in view of Nalbantis and further in view of Richard et al. (US 6,894,266) (Richard). Claims 5-6 have been rejected under § 103 as being unpatentable by Blake in view of Nalbantis and further in view of Collins et al. (US 5,724,009) (Collins). Claim 21 has been rejected under § 103 as being unpatentable by Blake in view of Nalbantis and Tomasz, and further in view of Collins.

### **Formalities**

Several claim amendments have been made, but not in response to any rejections. Various dependent claims have been amended to depend from non-canceled parent claims. Claim 3 has been amended to conform to the language of amended claim 1. Claim 21 has been amended to make the language consistent throughout claim 21. In line 3 of claim 30, "connected" has been replaced by "coupled."

### **Prior Art Rejections**

Amended claim 1 recites an RF power amplifier formed using an integrated circuit having a plurality of interface pins, comprising "a power amplifier circuit," "a mode selection pin for selecting a first mode or a second mode of operation," "a first interface pin, wherein the first

interface pin has a first function in the first mode of operation and a second function in the second mode of operation," and "a serial interface formed using the integrated circuit for sending and receiving signals."

Blake discloses a programmable gain amplifier. Blake shows an op-amp 102 formed on an integrated circuit 100. The integrated circuit 100 includes a serial peripheral interface 106. Blake does not teach or suggest a mode selection pin that is used to select first or second mode of operation. In addition, Blake does not teach or suggest an interface pin that has different functions in first and second modes of operation. An advantage of one example of a power amplifier of the present invention is that it can operate in different modes, where one or more pins have different functions, depending on the mode selected. For example, FIG. 2 of the present application illustrates various interface pins, and shows functions of the pins for different modes. For example, one pin is shown as being used as a serial data input (SDI) pin in one mode, and as a voltage reference (VDD) pin in another mode. Of course, these are just examples, and the claims are not limited to the examples shown in the figures.

In the Office Action, when discussing claims 2, 41, and 42, the Office Action alleges that Blake "teaches a chip select CS pin for controlling functions either in the 'shifting data' mode or in the 'latching' data mode," and that the chip select CS pin would act as the mode control pin SEN taught by Nalbantis. First, assuming that the chip select CS pin of Blake is used as a "chip select" input in the conventional sense, the purpose of the chip select CS pin is to tell the chip when input changes (e.g., in serial data input SI) are meant for it, versus other chips. If CS changes states, the functions of the interface pins remain the same (e.g., SI is still a serial data input pin, SO is still a serial data output pin, and SCK is still a serial clock input pin). Likewise, in Nalbantis, the SEN signal merely tells the shift register 42 whether to store or shift bits in

response to a transition of the serial clock SCLK. Like with Blake, when SEN changes states, the functions of the interface pins remain the same (e.g., SDATA is still a serial data input pin and SCLK is still a serial clock input pin).

For at least these reasons, applicant asserts that amended claim 1 is allowable over the prior art. Since dependent claims 3-6 depend from amended claim 1, it is also believed that these claims are allowable over the prior art.

Amended claim 14 recites a wireless communication device comprising "a controller circuit adapted to control the operation of the communication device," "a transceiver," "an RF power amplifier having a mode control pin and a first interface pin, wherein the state of the mode control pin determines whether the RF power amplifier operates using a serial interface mode or a pin control mode, and wherein the first interface pin has a first function in the serial interface mode and a second function in the pin control mode," and "a serial bus coupled to the controller, transceiver, and RF power amplifier."

For at least the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 14 is allowable over the prior art. Since dependent claims 18 and 21 depend from amended claim 14, it is also believed that these claims are allowable over the prior art.

Amended claim 30 recites a method of controlling an RF power amplifier in a wireless communications device, comprising "providing a baseband controller coupled to a digital bus," "providing an RF power amplifier having a serial interface for communicating with the digital bus and having a mode control pin," "applying a control signal to the mode control pin to select between a first mode of operation and a second mode of operation," "providing a first interface pin, wherein the first interface pin has a first function in the first mode of operation and a second

function in the second mode of operation," and "coupling the serial interface of the RF power amplifier to the digital bus."


For at least the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 30 is allowable over the prior art. Since dependent claims 42-45 depend from amended claim 30, it is also believed that these claims are allowable over the prior art.

#### Conclusion

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible. Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 to deposit account number 50-3864 (Johnson & Associates).

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Date

Respectfully Submitted,

  
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